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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/631,061	07/31/2003	Thomas R. Forrer JR.	AUS920030307US1	3511

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EXAMINER	
BATAILLE, PIERRE MICHE	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/631,061	FORRER ET AL.	
	Examiner	Art Unit	
	Pierre-Michel Bataille	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-48 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,052,798 (Jeddeloh).

3. With respect to claims 1, 17, and 33, Jeddeloh discloses a computer program/method in a data processing system including a storage drive for verifying a condition of said storage drive's media, comprising:

A) receiving within said storage drive a command to verify said condition of said storage drive's media ***(step 64, a memory access request is received from a memory requester, such as the system processor)***;

B) in response to a receipt of said command, attempting, by said storage drive, to read each one of a plurality of logical block addresses included in said storage drive ***(the memory access request to include an indication of whether a read or a write is being requested together with an address of the requested memory portion of the memory block)***; and

C) verifying said condition of said media by determining, by said storage drive, ones of said plurality of logical block addresses that are not in a readable

condition ***(step 66 determines whether the requested memory portion of the memory block is defective) [See steps 64 and 66, Fig. 3; Col. 5, Lines 51-61].***

4. With respect to claims 2, 18, and 34, Jeddeloh discloses reassigning each one of said ones of said plurality of logical block addresses that are not in a readable condition to a new logical block address ***[(mapping the defective memory portions determined in step 50 to non-defective memory portions in the reserved memory region) Step 60, Fig. 2; Col. 5, Lines 41-43]***.

With respect to claims 3, 19, and 35, Jeddeloh discloses:

A) determining, by said storage drive, ones of said plurality of logical block addresses that are nonreadable ***(determining defective memory portions; step 50, Fig. 2)***;

B) determining whether nonreadable logical block addresses are to be reassigned ***[Col. 5, Lines 20-27]***;

C) in response a determination that nonreadable logical block addresses are not to be reassigned, leaving said ones of said plurality of logical block addresses that are nonreadable unaltered without reassigning said ones of said plurality of logical block addresses that are nonreadable ***[Col. 5, Lines 26-34]***; and

D) in response to a determination that nonreadable logical block addresses are to be reassigned, reassigning said ones of said plurality of logical block addresses that are nonreadable ***[Col. 5, Lines 20-34]***.

5. With respect to claims 4, 20, and 36, Jeddeloh discloses determining whether nonreadable logical block addresses are to be reassigned by checking the status of a parameter, said parameter indicating whether nonreadable logical block addresses are to be reassigned ***(checking the error map to determine whether logical blocks are to be reassigned) [Col. 5, Lines 15-34; Fig. 2]***.

6. With respect to claims 5, 21, and 37, Jeddeloh discloses receiving within said storage drive a single command to verify said condition of said storage drive's media ***[Col. 5, Lines 52-59].***

7. With respect to claims 11, 27, and 39, Jeddeloh discloses during said verification, maintaining a list of said ones of said plurality of logical block addresses that are not in a readable condition ***[Col. 3, Lines 49-59]***.

8. With respect to claims 12, 28, and 44, Jeddeloh discloses verifying said condition of said media without altering data stored on said storage drive ***[Col. 4, Lines 31-41]***.

9. With respect to claims 13, 29, and 45, Jeddeloh discloses verifying said condition of said media without altering customer data stored on said media ***[Col. 4, Lines 14-41; Col. 5, Lines 15-34]***.

10. With respect to claims 14, 30, and 46, Jeddeloh discloses said storage drive being coupled to a host computer system; querying said storage drive by said host computer system during said verification; and transmitting a response to said query from said storage device to said host computer system during said verification ***[Col. 4, Lines 31-41; Col. 5, Lines 15-34]***.

11. With respect to claims 15, 31, and 47, Jeddeloh discloses querying said storage drive by said host computer system during said verification, said query requesting a completion status; and transmitting a percentage completion from said storage device to said host computer system during said verification ***[Col. 4, Lines 5-48]***.

12. With respect to claims 16, 32, and 48, Jeddeloh discloses querying said storage drive by said host computer system during said verification, said query requesting a list of reassigned logical block addresses; and transmitting said list from said storage device to said host computer system during said verification ***[Col. 5, Lines 15-34; Col. 6, Lines 9-23]***.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 6-9, 22-25, and 38-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052,7987 (Jeddeloh) in view of US 4,864,532 (Reeve et al).

15. With respect to claims 6-8, 22-24, and 38-40, Jeddeloh discloses

A) the memory device being nonvolatile memory such as EEPROM or flash memory [Col. 3, Lines 6-10; Col. 3, Lines 41-45] the memory being coupled through memory and expansion bus 26, Fig. 2; but fails to specifically teach coupling and decoupling itself from the host.

B) However, Reeve discloses sequence of operations operated in the sequential handling of data transfer operations where disk drive reconnects and disconnects itself to/from to data link processor in the process of transferring data complete I/O cycled operations [Col. 12, Lines 4-31]. Therefore, it would have been obvious to one of ordinary skill in the art, that storage medium couples and decouples itself from the host, as taught by Reeve, in order to continue an operation which was previously started by the data link processor.

16. With respect to claims 9, 25, and 41, Jeddeloh Jeddeloh discloses

A) the memory device being nonvolatile memory such as EEPROM or flash memory [Col. 3, Lines 6-10; Col. 3, Lines 41-45] the memory being coupled through memory and expansion bus 26, Fig. 2; but fails to specifically teach coupling said storage drive to a host utilizing a SCSI bus.

B) However, Reeve discloses sequence of operations operated in the sequential handling of data transfer operations Small computer systems interface (SCSI) bus [abstract; title]. Therefore it would have been obvious to one of ordinary skill in the art, to utilize SCSI bus, as taught by Reeve, because SCSI controls information transfer between a host computer system and certain compatible target devices.

17. Claims 10, 26, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6052,7987 (Jeddeloh) in view of US 6,332,204 (Russell).

With respect to claims 10, 26, and 42, Jeddeloh discloses the use of an error table to reassign logical block addresses; but fails to specifically teach determining block addresses that require error recovery procedures. However, Russell discloses determining logical block addresses that require error recovery procedures and reassigning block addresses that require error recovery procedures [abstract; Col. 2, Lines 22-26]. Therefore, it would have been obvious to one of ordinary skill in the art, to recover failing sectors because data within a failing sector could be recovered before the sector becomes completely unrecoverable, as taught by Russell [Col. 2, Lines 26-29].

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,332,204 (Russell) teaches recovering and relocating unreliable disk sectors when encountering disk drive read errors.

US 5,778,167 Carrel et al) teaches system and method for reassigning a storage location for reconstructed data on a persistent medium storage system.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (571) 272-4178. The examiner can normally be reached on Mon-Fri (8:00A to 4:30P).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Pierre-Michel Bataille
Primary Examiner
Art Unit 2186

December 8, 2005

PIERRE BATAILLE
PRIMARY EXAMINER